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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/023,819	12/21/2001	Biju Chandran	219.40779X00	3133

20457 7590 05/06/2003

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EXAMINER	
VIGUSHIN, JOHN B	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 05/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/023,819	Applicant(s) CHANDRAN ET AL.
	Examiner John B. Vigushin	Art Unit 2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-13* is/are allowed.

6)☒ Claim(s) *14-16,20-24,28 and 29* is/are rejected.

7)☒ Claim(s) *17-19 and 25-27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *0403a* .

4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other:

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

On p.14, line 8: "with" should be changed to --within--.

Appropriate correction is required.

Rejections Based On Prior Art

2. The following references were relied upon for the rejections hereinbelow:

Bernier et al. (US 2002/0195707 A1)   Dauksher et al. (US 6,320,754 B1)

Jimarez et al. (US 6,191,952 B1)

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 14-16, 21-24 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dauksher et al. and Jimarez et al. (not used as a secondary reference but rather as an evidentiary reference for showing that the conventional semiconductor IC chips used in Dauksher et al. have a CTE range of about 3 to 6 ppm/°C).

A) As to Claim 14:

I. Dauksher et al. discloses, in Fig. 5a: a substrate (i.e., a PC board) 504 having a first coefficient of thermal expansion (CTE) (col.3: 55-57); a semiconductor IC chip 502 having a second CTE which is different than the first CTE (col.1: 41-43); a plurality of soldered joints connecting chip 502 and substrate 504 (col.1: 46-49); chip 502 and substrate 504 across the respective soldered joints of the assembly at room temperature have CTE induced elongation mismatches from soldering (col.1: 39-59); the magnitude of the elongation mismatches are less than that expected based upon cooling substrate 504 and chip 502 from the solder solidification temperature to room temperature following soldering of the soldered joints (col.3: 41-43 and 23-40).

II. Dauksher et al. provides exemplary data showing how an annular ring 506 applied to an alumina (Al_2O_3) IC package 508 (Fig. 5b) reduces the CTE induced elongation mismatches from soldering between the alumina package 508 and substrate 504 (col.3: 44-col.6: 61): In particular, Dauksher et al. discloses the use of and experimental data relating to the annular ring 506 assembled to the IC chip 502 for a direct chip attachment to substrate 504 (Fig. 5a; col.3: 23-40) **but does not provide any exemplary experimental data for said direct chip attachment embodiment and consequently does not teach the limitation "wherein the magnitude of the elongation mismatches are less than one-half that expected based upon cooling the substrate and semiconductor chip from the solder solidification temperature to room temperature following soldering of the soldered joints.**"

III. However, Dauksher et al. discloses, in the alumina package exemplary experiment, that said alumina package 508 has a CTE of 6ppm/°C (col.3: 52-53). Now, evidently, Dauksher et al. is using a conventional semiconductor IC chip (col.1: 13-16 and 35-39), and it is old and well-known in the art, as evidenced by Jimarez et al. (col.3: 9-11), that conventional chip materials have CTEs of about 3 to 6ppm/°C. Furthermore, the annular ring 506, disclosed in Dauksher et al., is made of some material that has a higher CTE than the chip 502 (col.3: 10-12) which, evidently, can be selected in accordance with the assembly materials and requirements for a particular application (e.g., ring 506 can be made of aluminum for use in the mounting of the exemplary alumina IC package 508 to the PC substrate 504; Fig. 5b and col.3: 52-57), the disclosed use of ring 506 results in CTE induced elongation mismatches (manifested, *inter alia*, in solder joint shear) that are **less than one-half** of those that occur without the use of ring 506 due to the cooling of substrate 504 and alumina IC package 508 from the solder solidification temperature to room temperature (col.3: 23-43); e.g., CTE induced elongation mismatch in the form of solder joint shear is -0.0508 **<u>with</u>** the use of ring 506, which is **less than one-half** the solder joint shear--i.e., less than one-half of the expected value -0.73 based upon cooling the Fig. 5a assembly from the solder solidification temperature to room temperature following soldering the soldered joints--without the use of ring 506 (col.5: 44-55). Since the alumina IC package 508 of the exemplary experimental embodiment in Fig. 5b and col.3: 44-col.6: 61 is 6ppm/°C (which is very close to the chip 502 CTE of 3 to 6ppm/°C), then it would have been readily recognized in the pertinent art of Dauksher et al. that a ring 506 of appropriate

dimensions and material could be selected for use with chip 502 such that the chip solder joints would also exhibit a shear that is less than one-half the chip solder joint shear without the use of the ring (due to the cooling of substrate 504 and chip 502 from the solder solidification temperature to room temperature; col.3: 23-43), analogous to the above-mentioned reduction of solder joint shear in the solder joints of alumina substrate IC package 508 in the exemplary embodiment disclosed in col.5: 44-col.6: 55.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select the dimensions and material of the annular ring 506 for use with chip 502 such that the CTE induced elongation mismatch, manifested in solder joint shear, is less than one-half that expected based upon cooling the substrate 504 and chip 502 without the use of the annular ring 506, in order to prolong the solder joint fatigue life, hence, enhance reliability of the Fig. 5a chip-to-substrate assembly.

B) As to Claim 15, Dauksher et al. further discloses that the elongation mismatches are reflected in residual plastic deformation in the soldered joints and in post soldering residual stress (col.5: 44-55; col.3: 36-39).

C) As to Claim 16, Dauksher et al. discloses a conventional semiconductor IC chip 502, as discussed above (see the rejection of Claim 14), and evidentiary reference Jimarez et al. indicates that conventional chips have CTEs of about 3 to 6ppm/°C, also indicated in the rejection of base Claim 14, above. Since Dauksher et al. discloses that PC substrate 504 has a CTE of 17.6 ppm/°C (col.3: 55-57), then, inherently, first CTE

17.6 ppm/°C of substrate 504 is more than two times greater than second CTE, say the upper range value 6 ppm/°C, of chip 502.

As to Claim 21, the plurality of soldered joints each comprise solder on the semiconductor chip which is wetted onto a surface of the substrate to form the soldered joint (Fig. 5a; col.3: 23-43 and, analogous to the alumina IC package solder joints of Fig. 5b, col.3: 46-50).

As to Claim 22:

I. Dauksher et al. discloses, in Fig. 5a: a package substrate (i.e., a PC board) 504 having a first coefficient of thermal expansion (CTE) of at least 15 ppm/°C (specifically, 17.6 ppm/°C; col.3: 55-57), the package having a plurality of contact members (not shown, but inherently present on the surface of package substrate 504 for receiving the chip solder balls in Fig. 5a); a semiconductor IC chip 502 having a second CTE, unspecified, which is different than the first CTE (col.1: 41-43): Moreover, Dauksher et al. evidently is using a conventional semiconductor IC chip (col.1: 13-16 and 35-39), and it is old and well-known in the art, as evidenced by Jimarez et al. (col.3: 9-11), that conventional chip materials have CTEs of about 3 to 6 ppm/°C, and that being the case, then chip 502 inherently has a CTE which is at least 2.7 ppm/°C less than the CTE (17.6 ppm/°C) of package substrate 504; a front side of chip 502 having solder connections thereon (Fig. 5a), chip 502 being located on package substrate 504 with the solder connections connected to respective ones of the contact members by soldered joints electrically coupling chip 502 to package substrate 504 (Fig. 5a; col.3: 38-39); a plurality of soldered joints connecting chip 502 and package substrate 504

(col.1: 46-49); chip 502 and package substrate 504 across the respective soldered joints of the assembly at room temperature have CTE induced elongation mismatches from soldering (col.1: 39-59); the magnitude of the elongation mismatches are less than that expected based upon cooling package substrate 504 and chip 502 from the solder solidification temperature to room temperature following soldering of the soldered joints (col.3: 41-43 and 23-40).

II. Dauksher et al. provides exemplary data showing how an annular ring 506 applied to an alumina (Al_2O_3) IC package 508 (Fig. 5b) reduces the CTE induced elongation mismatches from soldering between the alumina package 508 and package substrate 504 (col.3: 44-col.6: 61): In particular, Dauksher et al. discloses the use of and experimental data relating to the annular ring 506 assembled to the IC chip 502 for a direct chip attachment to package substrate 504 (Fig. 5a; col.3: 23-40) **but does not provide any exemplary experimental data for said direct chip attachment embodiment and consequently does not teach the limitation "wherein the magnitude of the elongation mismatches are less than one-half that expected based upon cooling the substrate and semiconductor chip from the solder solidification temperature to room temperature following soldering of the soldered joints**."

III. However, Dauksher et al. discloses, in the alumina package exemplary experiment, that the alumina package 508 has a CTE of 6ppm/°C (col.3: 52-53). Now, evidently, Dauksher et al. is using a conventional semiconductor IC chip (col.1: 13-16 and 35-39), and it is old and well-known in the art, as evidenced by Jimarez et al. (col.3:

9-11), that conventional chip materials have CTEs of about 3 to 6 ppm/°C. Furthermore, the annular ring 506, disclosed in Dauksher et al., is made of some material that has a higher CTE than the chip 502 (col.3: 10-12) which, evidently, can be selected in accordance with the assembly materials and requirements for a particular application (e.g., ring 506 can be made of aluminum for use in the mounting of the exemplary alumina IC package 508 to the PC substrate 504; Fig. 5b and col.3: 52-57), the disclosed use of ring 506 results in CTE induced elongation mismatches (manifested, *inter alia*, in solder joint shear) that are less than one-half of those that occur without the use of ring 506 due to the cooling of package substrate 504 and alumina IC package 508 from the solder solidification temperature to room temperature (col.3: 23-43); e.g., CTE induced elongation mismatch in the form of solder joint shear is -0.0508 **with** the use of ring 506, which is less than one-half the solder joint shear--i.e., less than one-half of the expected value -0.73 based upon cooling the Fig. 5a assembly from the solder solidification temperature to room temperature following soldering the soldered joints--without the use of ring 506 (col.5: 44-55). Since the alumina IC package 508 of the exemplary experimental embodiment in Fig. 5b and col.3: 44-col.6: 61 is 6ppm/°C (which is very close to the chip 502 CTE of 3 to 6ppm/°C), then it would have been readily recognized in the pertinent art of Dauksher et al. that a ring 506 of appropriate dimensions and material could be selected for use with chip 502 such that the chip solder joints would also exhibit a shear that is less than one-half the chip solder joint shear without the use of the ring (due to the cooling of package substrate 504 and chip 502 from the solder solidification temperature to room temperature; col.3: 23-43),

analogous to the above-mentioned reduction of solder joint shear in the solder joints of alumina substrate IC package 508 in the exemplary embodiment disclosed in col.5: 44-col.6: 55.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select the dimensions and material of the annular ring 506 for use with chip 502 such that the CTE induced elongation mismatch, manifested in solder joint shear, is less than one-half that expected based upon cooling the package substrate 504 and chip 502 without the use of the annular ring 506, in order to prolong the solder joint fatigue life, hence, enhance reliability of the Fig. 5a chip-to-substrate assembly.

As to Claim 23, Dauksher et al. further discloses that the elongation mismatches are reflected in residual plastic deformation in the soldered joints and in post soldering residual stress (col.5: 44-55; col.3: 36-39).

As to Claim 24, Dauksher et al. discloses a conventional semiconductor IC chip 502, as discussed above (see the rejection of Claim 14), and evidentiary reference Jimarez et al. indicates that conventional chips have CTEs of about 3 to 6ppm/°C, also indicated in the rejection of base Claim 22, above. Since Dauksher et al. discloses that PC substrate 504 has a CTE of 17.6 ppm/°C (col.3: 55-57), then, inherently, first CTE 17.6 ppm/°C of substrate 504 is more than two times greater than second CTE, say the upper range value 6 ppm/°C, of chip 502.

As to Claim 29, Dauksher et al. further discloses that the plurality of soldered joints each comprise solder on the semiconductor chip which is wetted onto a surface of

the substrate to form the soldered joint (Fig. 5a; col.3: 23-43 and, analogous to the alumina IC package solder joints of Fig. 5b, col.3: 46-50).

5. Claims 20 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dauksher et al. and Jimarez et al. in view of Bernier et al.

As to Claims 20 and 28:

I. Modified Dauksher et al. and Jimarez et al. disclose all the limitations of base Claims 14 and 22 including the semiconductor chip 502 joined by soldered joints to substrate 504 along chip 502 (Fig. 5a; col.1: 46-49). Dauksher et al. does not teach that semiconductor chip 502 is joined by soldered joints to substrate 504 along chip 502 **over a distance of at least 4mm from the center of the chip**.

II. Bernier et al. teaches a semiconductor chip 12 joined by soldered joints 16 to substrate 14 along chip 12 (Fig. 1; paragraph [0026]) over a distance of at least 4mm from the center of the chip (Fig. 3) wherein the solder shear and axial strains are greater and potentially damaging to the package at solder joint distances greater than 4 mm from the center of chip 12, the higher values of shear and axial strain at distances greater than 7 mm varying at certain distances from edge 13 of chip 12 (Figs. 3 and 4; p.3: paragraphs [0043] and [0044]). The shear and axial strain are due to CTE mismatches between chip 12 and substrate 14 as well as CTE mismatches between solder 16 and chip 12, and solder 16 and substrate 14 (p.2: paragraph [0032]).

III. Since Bernier et al. (see Fig. 3) discloses problematic, package-damaging solder shear increases in solder ball connections along the chip over 4mm from the center of the chip, and Dauksher et al. (see Fig. 5a, col.3: 23-40 and col.5: 44-55)

discloses minimizing the CTE induced elongation mismatch problems--one of which, is manifested in the form of damaging shear forces in the solder joint connections--by means of the annular ring 506 around chip 502, then it would have been obvious to one of ordinary skill in the art at the time the invention was made to join semiconductor chip 502 (framed by annular ring 506) by the solder joints to substrate 504 along chip 502 over a distance of at least 4mm from the center of the chip in order to greatly reduce the solder joint shear in the solder joints of chip 502 (see Dauksher et al., col.5: 44-55), especially those solder joints that are located over a distance 4 mm from the center of the chip where the solder joint shear forces are greatest, as taught by Bernier et al.

Allowable Subject Matter

6. Claims 1-13 have been allowed.

7. Claims 17-19 and 25-27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter:

As to Claims 1-9, patentability resides in *thermally expanding each of the semiconductor chip and substrate substantially the same amount in direction along surfaces thereof to be joined by soldering*, in combination with the other limitations of base Claim 1.

As to Claims 10-13, patentability resides in *thermally expanding each of the first and second members substantially the same amount in a direction along surfaces thereof to be joined*, in combination with the other limitations of base Claim 10.

As to Claims 17-19 and 25-27, patentability resides in *the limitation wherein the soldered joints connect the semiconductor chip to the tops of respective ones of the standoff elements*, in combination with the other limitations of the broadest claims, Claims 17 and 25.

9. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Sylvester (US 6,014,317) discloses, in Fig. 18, that the CTE induced elongation mismatch between chip 124 and substrate 126, causing die and substrate warpage, is zeroed by the equal and opposite bending moments of chip 124 and opposing false die 132 that essentially cancel the CTE induced elongation mismatch (col.19: 5-57).

b) Iijima et al. (US 2001/0008309 A1) discloses compliant standoffs 208 on substrate 211 for reducing the effects of the CTE induced elongation mismatch between

chip 205 and substrate 211 during the cooling of the package following the reflow of solder joints 207 (Figs. 3, 4, 5A,B; paragraphs [0112] and [0116]).

c) Downes (US 6,222,277 B1) discloses high temperature solder balls 40, 42 (i.e., "standoffs") positioned along selected locations along the periphery of the substrate for reducing the effects of the CTE induced elongation mismatch (i.e., mechanical stresses in solder joints 41) between chip 10 and substrate 20 (Figs. 5 and 6; col.10: 1-21).

d) Kutlu (US 6,472,762 B1) discloses a package wherein the CTE of the combined heatspreader 104 and die 102 assembly is adjusted to match the CTE of substrate 106 in order to, *inter alia*, eliminate solder joint stress and prevent warpage and cracking of die 102 and substrate 106 (col.2: 3-22 and 56-59).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 703-308-1205. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on 703-305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7382 for regular communications and 703-308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

John B. Vigushin
John B. Vigushin
Examiner
Art Unit 2827

jbv
April 29, 2003